CLAIMS

What is claimed is:

1. A method for operating a phase-locked loop (PLL), said method comprising:

providing a control current; and

varying the control current in proportion to the inverse of *N* squared, wherein *N* is a ratio of an output frequency of the PLL to a reference frequency of the PLL, wherein varying the control current compensates for bandwidth changes of the PLL.

2. The method of claim 1, wherein varying includes varying a magnitude of the control current.

3. The method of claim 1, wherein varying includes altering current flow provided by at least one current source, wherein the at least one current source provides the control current.

4. The method of claim 3, wherein the at least one current source is disposed in a charge pump, the charge pump disposed in the PLL.

5. The method of claim 3, further including receiving a value of *N*, wherein the altering is based on the value of *N*.

6. A method for operating a phase-locked loop (PLL), said method comprising:

providing a detector; and

varying the gain of the detector in proportion to the inverse of *N* squared, wherein *N* is a ratio of an output frequency of the PLL to a reference frequency of the PLL, wherein varying the gain of the detector compensates for bandwidth changes of the PLL.

7. The method of claim 6, wherein the detector includes at least one of a phase detector and a frequency detector.

8. A method for operating a phase-locked loop (PLL), said method comprising:

providing a control signal;

receiving state information, the state information corresponding to tuning information;

multiplying the control signal by a square root of the state information to provide a tuning signal; and

providing the tuning signal to a capacitor array, the capacitor array comprising a weighted variable capacitor and a weighted switched capacitor.

9. The method of claim 8, wherein the weighted variable capacitor and the weighted switched capacitor array are binary weighted.

10. The method of claim 8, wherein the control signal is provided by a charge pump through a low pass filter.

11. The method of claim 8, wherein the state information is provided by a frequency control circuit.

12. The method of claim 8, wherein the capacitor array is disposed in an oscillator, the oscillator located in the PLL.

13. The method of claim 8, wherein the multiplying is performed in a square root module.

14. A phase-locked loop (PLL), comprising:

a current generating device configured to generate a control current; and

a switching module configured to vary the control current in proportion to the inverse of N squared, wherein N is a ratio of an output frequency of the PLL to a reference frequency of the PLL.

15. The phase-locked loop of claim 14, wherein the current generating device includes at least one current source and at least one switch that controls the flow through the at least one current source.

16. The phase-locked loop of claim 15, wherein the switching module is configured to activate the at least one switch based on a value of *N* programmed into the PLL.

17. The phase-locked loop of claim 15, wherein the switching module is configured to activate the at least one switch based on a threshold range of *N*.

18. The phase-locked loop of claim 14, wherein the current generating device is a charge pump.

19. The phase-locked loop of claim 18, further including a loop filter, an oscillator, a divide-by-*N* module, and a phase/frequency detection device, wherein the loop filter is disposed between the charge pump and the oscillator, the divide-by-*N* module is disposed between the oscillator and the phase/frequency device, the phase/frequency device is coupled to the charge pump.

20. The phase-locked loop of claim 19, wherein the charge pump, the loop filter, the oscillator, the divide-by-*N* module, and the phase/frequency detection device are disposed on a single semiconductor chip.

21. A phase-locked loop (PLL), comprising:

a detector; and

a switching module configured to vary the gain of the detector in proportion to the inverse of *N* squared, wherein *N* is a ratio of an output frequency of the PLL to a reference frequency of the PLL.

22. The phase-locked loop of claim 21, wherein the detector includes one of a phase detector and a frequency detector.

23. The phase-locked loop of claim 22, further including a loop filter, an oscillator, and a divide-by-*N* module, the loop filter disposed between the detector and the oscillator, the divide-by-*N* module disposed between the oscillator and the detector.

24. The phase-locked loop of claim 23, wherein the loop filter, the oscillator, the divide-by-*N* module, and the detector are disposed on a single semiconductor chip.

25. A phase-locked loop (PLL), comprising:

a signal device configured to provide a control signal; and

a square root module configured to receive state information, the state information corresponding to tuning information, the square root module further configured to multiply the control signal by a square root of the state information to provide a tuning signal.

26. The phase-locked loop of claim 25, further including an oscillator having a capacitor array, the oscillator coupled to the square root module, the capacitor array comprising at least one weighted variable capacitor and at least one weighted switched capacitor.

27. The phase-locked loop of claim 26, wherein the oscillator is configured to receive the tuning signal such that the capacitor array is tuned.

28. The phase-locked loop of claim 26, wherein the at least one weighted variable capacitor and at least one weighted switched capacitor array are binary weighted.